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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,126	02/11/2004	Hidenori Yato	118425	2452

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EXAMINER	
VU, HUNG K	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,126	YATO, HIDENORI	
	Examiner	Art Unit	
	Hung Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-5 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-5 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/11/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Miida (PN 6,504,194).

Miida discloses, as shown in Figures 2A, a solid-state imaging device, comprising:

a pixel array having a plurality of unit pixels, each of the unit pixels including a photo diode (111) and an insulated gate field effect transistor (112) that detects photocharges;

a control circuit that controls the operation of the pixel array [Figure 8], wherein:

the photo diode and the insulated gate field effect transistor share a well region (15a,15b) of a first conductivity type (p type) that is formed in a semiconductor layer (12) of a second conductivity type (n type), the semiconductor layer of the second conductivity type being formed on a semiconductor substrate (11) of the first conductivity type (p type);

an accumulation region that accumulates charges of a given conductivity type generated in response to light incident on the photo diode that formed in the well region of the insulated gate field effect transistor;

the control circuit forward biases a junction region between the semiconductor substrate and the semiconductor layer so as t accumulated a predetermined amount of the charges of the

given conductivity type in the accumulation region, and discharges the charges of the given conductivity type accumulated in the accumulation region thereafter.

Regarding claim 2, Miida discloses the insulated gate field effect transistor further comprising:

a source diffused region (16a) of the second conductivity type (n-type) formed on a surface of the well region;

a drain diffused region (17a) of the second conductivity type formed on a surface of the semiconductor layer other than the surface of the well region;

a gate electrode (19) formed above the well region between the drain diffused region and the source diffused region with a gate insulating film (18) therebetween;

a channel region (15c) formed in the surface of the well region below the gate electrode and having an impurity layer of the second conductivity type;

the accumulation region (25) being a heavily doped buried layer of the first conductivity type formed below the channel region n the well region and adjacent to the source diffused region, having impurity concentration higher than that of the well region;

the control circuit applied predetermined voltage to at least the drain diffused region to forward bias the junction region so as to accumulate a predetermined amount of the charges of the given conductivity type in the accumulation region, and discharges the charges of the given conductivity type accumulated in the accumulation region thereafter.

Regarding claim 3, Miida discloses a state where a predetermined amount of the charges of the given conductivity type are accumulated is a saturated state where a maximum amount of available charges of a given conductivity type are accumulated in the accumulation region.

Regarding claim 4, Miida discloses the charges of the given conductivity type being holes if the first conductivity type is a P type and the second conductivity type is an N type.

Regarding claim 5, Miida discloses the charges of the given conductivity type being electrons if the first conductivity type is a N type and the second conductivity type is an P type.

Conclusion

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

April 1, 2005

Hung Vu

Primary Examiner